CLAIMS

WHAT IS CLAIMED:

1.   A built-in self-test controller, comprising a logic built-in self-test domain capable of performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

2.   The built-in self-test controller of claim 1, wherein the logic built-in self-test domain comprises:
    a logic built-in self-test state machine; and
    a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.

3.   The built-in self-test controller of claim 2, wherein the logic built-in self-test state machine further comprises:
    a reset state entered upon receipt of an external reset signal;
    an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;
    a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;
    a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and
    a done state entered into from the step state when the content of the pattern generator equals the predetermined vector count.

4.   The built-in self-test controller of claim 2, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

5.   The built-in self-test controller of claim 2, wherein the logic built-in self-test signature includes at least one of:
    a bit indicating an error condition arose; and
    a bit indicating whether the stored results are from a previous logic built-in self-test run.

6.   The built-in self-test controller of claim 1, further comprising a memory built-in self-test domain.

7.   A built-in self-test controller, comprising a logic built-in self-test domain including means for performing a logic built-in self-test at a test frequency at least as slow as a slowest frequency of a plurality of timing domains to undergo the logic built-in self-test.

8.   The built-in self-test controller of claim 7, wherein the means for performing the logic built-in self-test comprises:
        a logic built-in self-test state machine; and
        a pattern generator capable of generating a scan pattern for use in a state of the logic built-in self-test state machine.

9.   The built-in self-test controller of claim 7, further comprising a memory built-in self-test domain.

10.   An integrated circuit device, comprising:
a plurality of memory components;
a logic core;
a testing interface; and
a built-in self-test controller controlled through the testing interface, comprising a
        logic built-in self-test domain capable of performing a logic built-in self-test at
        a test frequency at least as slow as a slowest frequency of a plurality of timing
        domains to undergo the logic built-in self-test.

11.   The integrated circuit device of claim 10, wherein the logic built-in self-test domain comprises:
        a logic built-in self-test state machine; and
        a pattern generator capable of generating a scan pattern for use in a state of the logic
                built-in self-test state machine.

12.   The integrated circuit device of claim 11, wherein the logic built-in self-test state machine further comprises:
        a reset state entered upon receipt of an external reset signal;

4   an initiate state entered from the reset state upon receipt of a logic built-in self-test run

5   signal;

6   a scan state entered from the initiate state upon the initialization of components and

7   signals in the logic built-in self-test domain in the initiate state;

8   a step state entered into from the scan state and from which the scan state is entered

9   unless the content of the pattern generator equals a predetermined vector

10   count; and

11   a done state entered into from the step state when the content of the pattern generator

12   equals the predetermined vector count.

1   13.   The integrated circuit device of claim 11, wherein the pattern generator

2   comprises a linear feedback shift register seeded with a primitive polynomial.

14.   The integrated circuit device of claim 11, wherein the logic built-in self-test

signature includes at least one of:

a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test

run.

15.   The integrated circuit device of claim 10, wherein the built-in self-test

controller further comprises a memory built-in self-test domain.

1   16.   The integrated circuit device of claim 10, wherein testing interface comprises

2   a Joint Test Action Group tap controller.

1   17.   An integrated circuit device, comprising:

2   a plurality of memory components;

3   a logic core;

4   a testing interface; and

5   means for performing a logic built-in self-test at a test frequency at least as slow as a

6   slowest frequency of a plurality of timing domains to undergo the logic built-

7   in self-test.

1   18.   The integrated circuit device of claim 17, wherein the performing means

2   comprises:

3   a logic built-in self-test state machine; and

4   a pattern generator capable of generating a scan pattern for use in a state of the logic

5   built-in self-test state machine.

1   19.   The integrated circuit device of claim 17, wherein the built-in self-test

2   controller further comprises a memory built-in self-test domain.

1   20.   The integrated circuit device of claim 17, wherein testing interface comprises

2   a Joint Test Action Group tap controller.

1   21.   A method for performing a built-in self-test on an integrated circuit device,

2   comprising:

3   externally resetting a built-in self-test controller including a logic built-in self-test

4   engine;

5   performing a logic built-in self-test from the built-in self-test controller at a test

6   frequency at least as slow as a slowest frequency of a plurality of timing

7   domains to undergo the logic built-in self-test; and

8   obtaining the results of the performed built-in self-test.

1   22.   The method of claim 21, wherein resetting the built-in self-test controller

     includes initializing a multiple input signature register and a pattern generator.

1   23.   The method of claim 21, wherein performing the logic built-in self-test

2   includes:

3   initiating a plurality of components and signals in a logic built-in self-test domain of

4   the dual mode built-in self-test controller upon receipt of a logic built-in self-

5   test run signal;

6   scanning a scan chain upon the initialization of the components and the signals;

7   stepping to a new scan chain; and

8   repeating the previous scanning and stepping until the content of a pattern generator

9   equals a predetermined vector count.

1   24.   The method of claim 23, further comprising at least one of:

2   setting a bit in the multiple input signature register indicating an error condition arose;

3   and

4 setting a bit in the multiple input signature register indicating whether the stored

5 results are from a previous logic built-in self-test run.

1 25. The method of claim 21, wherein externally resetting a built-in self-test

2 controller includes resetting a built-in self-test controller including a memory built-in self-test

3 engine and the method further comprises:

4 performing a memory built-in self-test from the built-in self-test controller; and

5 obtaining the results of the performed built-in self-test.

1 26. A method for testing an integrated circuit device, comprising:

2 interfacing the integrated circuit device with a tester;

3 externally resetting a built-in self-test controller including a logic built-in self-test

engine;

performing a logic built-in self-test from the built-in self-test controller at a test

frequency at least as slow as a slowest frequency of a plurality of timing

domains to undergo the logic built-in self-test; and

obtaining the results of the performed built-in self-test.

27. The method of claim 26, wherein resetting the built-in self-test controller

includes initializing a multiple input signature register and a pattern generator.

28. The method of claim 26, wherein performing the logic built-in self-test

2 includes:

3 initiating a plurality of components and signals in a logic built-in self-test domain of

4 the dual mode built-in self-test controller upon receipt of a logic built-in self-

5 test run signal;

6 scanning a scan chain upon the initialization of the components and the signals;

7 stepping to a new scan chain; and

8 repeating the previous scanning and stepping until the content of a pattern generator

9 equals a predetermined vector count.

1 29. The method of claim 28, further comprising at least one of:

2 setting a bit in the multiple input signature register indicating an error condition arose;

3 and

4   setting a bit in the multiple input signature register indicating whether the stored

5   results are from a previous logic built-in self-test run.

1   30.   The method of claim 26, wherein externally resetting a built-in self-test

2   controller includes resetting a built-in self-test controller including a memory built-in self-test

3   engine and the method further comprises:

4   performing a memory built-in self-test from the built-in self-test controller; and

5   obtaining the results of the performed built-in self-test. *Logic or memory?*

1   31.   The method of claim 26, wherein obtaining the results includes reading at least

2   one of a logic built-in self-test signature and a memory built-in self-test signature.

1   32.   The method of claim 26, wherein interfacing the integrated circuit device with

the tester includes employing Joint Test Action Group protocols.